reduced and the manufacturing cost for the dummy gate pattern for avoiding the proximity effect can be reduced.

Bothra teaches a method of manufacturing semiconductor devices with trenches that use a mask layer (col. 5, lines 13-25; Figure 3). However, Bothra does not teach a method of semiconductor manufacture that employs photolithography and two photomasks to determine the active and dummy regions and the active and dummy gates. Since the claimed process requires the use of two photomasks to manufacture the semiconductor device, and Bothra does not teach these steps, Bothra cannot be said to teach or render obvious claim 37 and the several claims dependent thereon, or claim 41.

In FIG. 2B of Bothra, a dummy active region 214 and a gate 226 are coupled between a power supply voltage and a ground voltage (see col. 5, lines 34-49). Neither Bothra nor Shimomura refer to the correction of the proximity effect.

In Bothra and Shimomura, since contacts are formed for applying voltages to a gate and impurity regions, it is impossible for form a gate pattern by simply shrinking patterns of the impurity regions. On the other hand, in the present claimed invention, since no voltage is required for the dummy gate patterns, the patterns of impurity regions are easily shrinked.

Additionally, in Bothra a mask for dummy active areas is independent of a mask for dummy gates, i.e. there is no relationship between the two masks.

In summary, Bothra and Shimomura never suggest the problem of or the solution of the present invention as defined by method claim 37, and the several claims dependent thereon, or claim 41.

Having dealt with all the objections raised by the Examiner, it is believed that the application now is in order for allowance. Early and favorable action are respectfully requested.

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In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our deposit account number 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: BOX RCE, Assistant Commissioner for Patents, Washington, D.C. 20231 on November 20, 2002, at Tucson, Arizona.

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MARKED SPECIFICATION PARAGRAPHS

SERIAL NO. 09/735,005

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MARKED SPECIFICATION PARAGRAPHS:

Paragraph beginning at page 3, line 13:

Figs. 3A, 3B and 3C are cross-sectional views for explaining a [first] second prior art method for manufacturing a semiconductor device;

Paragraph beginning at page 3, line 22:

Figs. 6A, 6B and 6C are diagrams for explaining a second step for designing a photomask used in [a] the first embodiment of the method for manufacturing a semiconductor device according to the present invention;

Paragraph beginning at page 4, line 24:

Finally, referring to Fig. 1C, the photoresist layer 103 is removed. Thus, the gate conductive layer 102 has gate patterns [G1] P1 and [G2] P2 corresponding to the gate patterns GP1 and GP2, respectively.